HMT7742 **Shortform** datasheet
GENIE IO-Link DEVICE SINGLE PHY

IO-Link

Features

The HMT7742 GENIE IO-Link DEVICE PHY is a transceiver between a microcontroller with a sensor or actuator function and a 24V power and signalling cable, specified to support IO-Link. Features include:

- integrated UART peripheral with M-sequence handling (inc. checksum) for all IO-Link specification 1.1 M-Sequences
- single octet UART mode for unlimited M-Sequence lengths.
- internal data buffer for up to 15 octets
- transparent UART mode for special applications
- IO-Link clock extraction and frame generation at 38.4kBaud and 230.4kBaud. No quartz required for communication.
- outputs configured to be high-side, low-side or push-pull (<10Ω)
- fast switching time (<1µs)
- configurable short circuit current limit and reporting
- zener limits for rapid inductive load switch off
- 5V to 35V supply range
- support for unequal supplies between the microcontroller and the HMT7742
- device reset reporting
- configurable 5V or 3.3V, 50mA linear regulator
- full zero current reverse polarity protection
- over-voltage protection to 35V
- configurable under-voltage detection
- ESD protection to 4kV
- EMC surge protection to IEC 60255-5 (2A/50µs)
- thermal shutdown, configurable level allows protection of neighbouring devices and packaging
- 7-bit, calibrated, temperature measurement
- two configurable current mode LED outputs
- Small format DFN 12LD 4mm x 3mm package

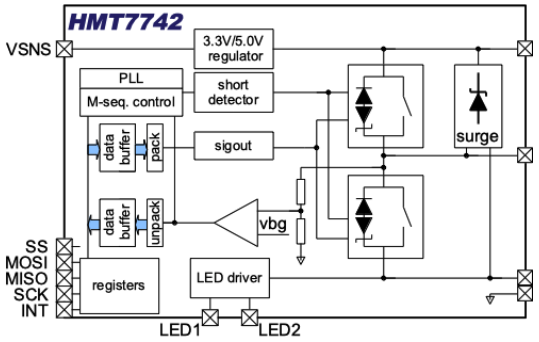
Functional Description

At start-up power is applied via the cable on VPLUS, and the microcontroller and sensor are supplied with a 3.3V or 5V supply from the HMT7742's linear regulator. On leaving reset the microcontroller proceeds to configure the HMT7742 to the desired operating mode.

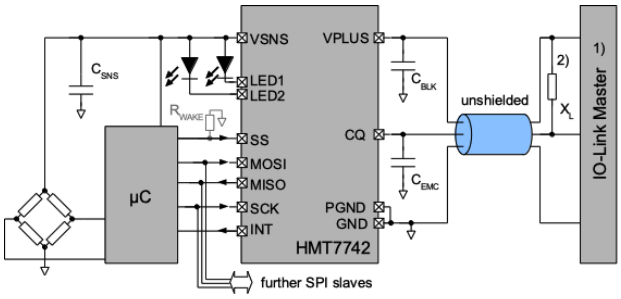
If the microcontroller places the HMT7742 into listen mode, or a wake-up request is generated by the IO-Link master, then the HMT7742 waits for an M-Sequence on the CQ line. Once this is received, its checksum and parity are checked by the HMT7742 and an interrupt is generated on INT.

The microcontroller now reads the data octets contained within the HMT7742's data buffers, and composes a return response in the HMT7742 via the SPI interface. The HMT7742 adds a parity and checksum and transmits the return frame on the CQ line, using a clock trimmed to the master clock.

In normal operation, the device may be run either in IO-Link mode, where data is transferred with UART frames, or in SIO



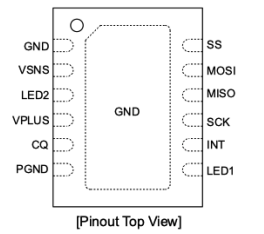
If the DUAL PHY is placed in listen mode, or receives a wake-up request from the IO-Link master, then the DUAL PHY waits for a UART frame on the CQ line. If one is received, its checksum and parity are checked by the DUAL PHY, and a interrupt is generated on INT.



1) Example sensor configuration shown
2) IO-Link master used for IO-Link mode device configuration
3) X_L (high- or low side) in Single Input Output mode. X_L has max reactive parts C_{LOAD_MAX} and I_{LOAD_MAX}

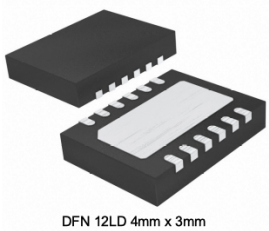
The microcontroller now reads the incoming frame, and composes a return frame via the SPI. The DUAL PHY adds parity and checksum and transmits the frame on the CQ line, using a clock trimmed to the master clock.

Package



[Pinout Top View]

NB: GND flag and GND pin to be connected on PCB



DFN 12LD 4mm x 3mm

Bare die available on request