HMT7748 **Shortform** datasheet
GENIE IO-Link DEVICE DUAL PHY

Features

The HMT7748 GENIE IO-Link DEVICE DUAL PHY is a transceiver between a microcontroller with a sensor or actuator function and a 24V power and signalling cable, specified to support IO-Link. Features include:

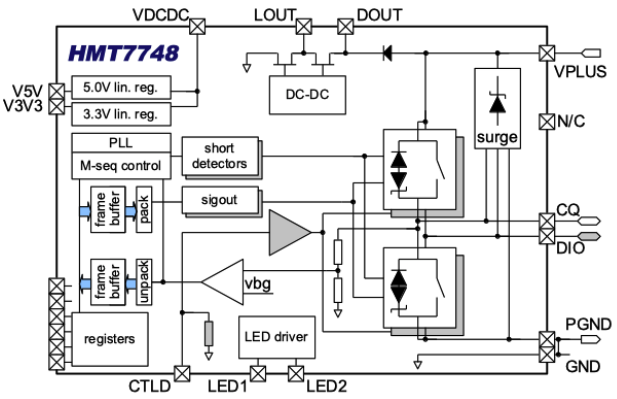
- integrated UART peripheral with M-sequence handling (inc. checksum) for all IO-Link M- Sequences
- internal data buffer for up to 15 octets
- single octet UART mode for unlimited M-sequence size and continuous data transfer
- transparent UART mode for special applications
- IO-Link clock extraction and frame generation at 38.4kBaud and 230.4kBaud. No quartz required for communication.
- **dual** outputs, configured to be high-side, low-side or push-pull (<10Ω)
- **configurable output doubling for additional drive strength requirements (nom. 500mA)**
- configurable short circuit current limit and reporting
- zener limits for rapid inductive load switch off
- 5V to 35V supply range
- 5V and 3.3V, 50mA linear regulators
- configurable frequency & voltage (4V-9V), 50mA DC-DC regulator
- **internal reverse polarisation diode** (DOUT pin)
- full zero current reverse polarity protection
- over-voltage protection to 35V
- configurable under-voltage detection
- ESD protection to 4kV
- EMC surge protection to IEC 60255-5 (2A/50µs)
- configurable thermal shutdown levels
- 7-bit, calibrated, temperature measurement
- two current mode LED outputs
- QFN 4x4 and CSP packages

Functional Description

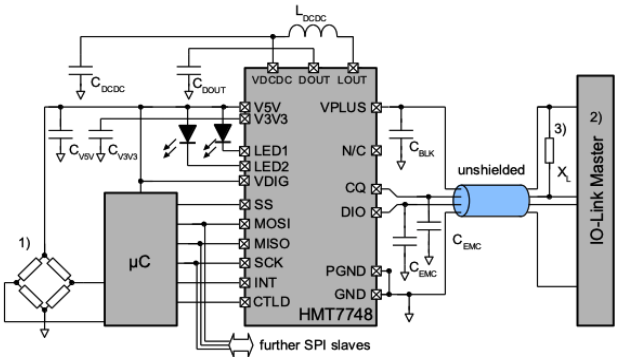
At start-up, power is applied via the cable on VPLUS and the device core is powered by the V3V3 supply from the linear **and dc-dc regulators.** On leaving reset the microcontroller proceeds to configure the DUAL PHY to the desired operating mode.

The DIO pin is a fully protected I/O which can be driven or sampled independently via SPI. With an external connection to CQ, it may also be used to provide a single output with doubled drive strength.

In operation, the device is run in IO-Link mode where data is transferred with UART frames, or in SIO mode where CQ is driven according to the sensor state.



If the DUAL PHY is placed in listen mode, or receives a wake-up request from the IO-Link master, then the DUAL PHY waits for a UART frame on the CQ line. If one is received, its checksum and parity are checked by the DUAL PHY, and a interrupt is generated on INT.



1) Example sensor configuration shown
2) IO-Link master used for IO-Link mode device configuration
3) X_L (high- or low side) in Single Input Output mode. X_L has max reactive parts C_{LOAD_MAX} and I_{LOAD_MAX}

The microcontroller now reads the incoming frame, and composes a return frame via the SPI. The DUAL PHY adds parity and checksum and transmits the frame on the CQ line, using a clock trimmed to the master clock.

Package