HMT7740/1 GENIE IO-Link DEVICE LIGHTWEIGHT PHY

The HMT7740 and HMT7741 GENIE family IC is a physical layer transceiver (PHY) with a simple and flexible switching architecture, comprised of two independently driven bi-directional floating switches, with integrated surge and zero current reverse polarity protection.

The device is primarily used in IO-Link or Single Input Output (SIO) switching applications for driving coils or inductive and capacitive loads for industrial sensor/actuator applications. The device is available in two voltage configurations, 3.3V (HMT7740) or 5.0V (HMT7741).

[1] This specification makes reference to IO-Link Interface and System Specification Version 1.1.3, June 2019

1.1 Features

- two switches independently driven (typ 3.5Ω)
- floating bidirectional switches, free selection of connection
- full zero current reverse polarity protection
- bidirectional short-circuit detection
- short circuit current limit auto-off/reporting/restart
- short circuit current derating with temperature
- fast demagnetisation of inductive loads
- fast switching time (<1µs)
- IO-Link level comparator (AA)
- 5V to 36V supply
- hot-plug protection
- thermal shutdown protection
- under-voltage detection
- ESD protection to ±4kV
- surge protection (±1kV/500Ω 1.2µs/50us) on any combination of high-voltage pins
- large inductive load compliance according to EN 60947-5-2 (DC13)
- 3.3V or 5V, 30mA linear regulator variants
- optimised for small designs
  - operation does not require micro-controller
  - operating current 2mA (max)
  - driver on resistance 3.5Ω (typ)
  - available in 3mm x 3mm DFN or 1.6mm x 2.6mm Chip Scale Package (CSP)

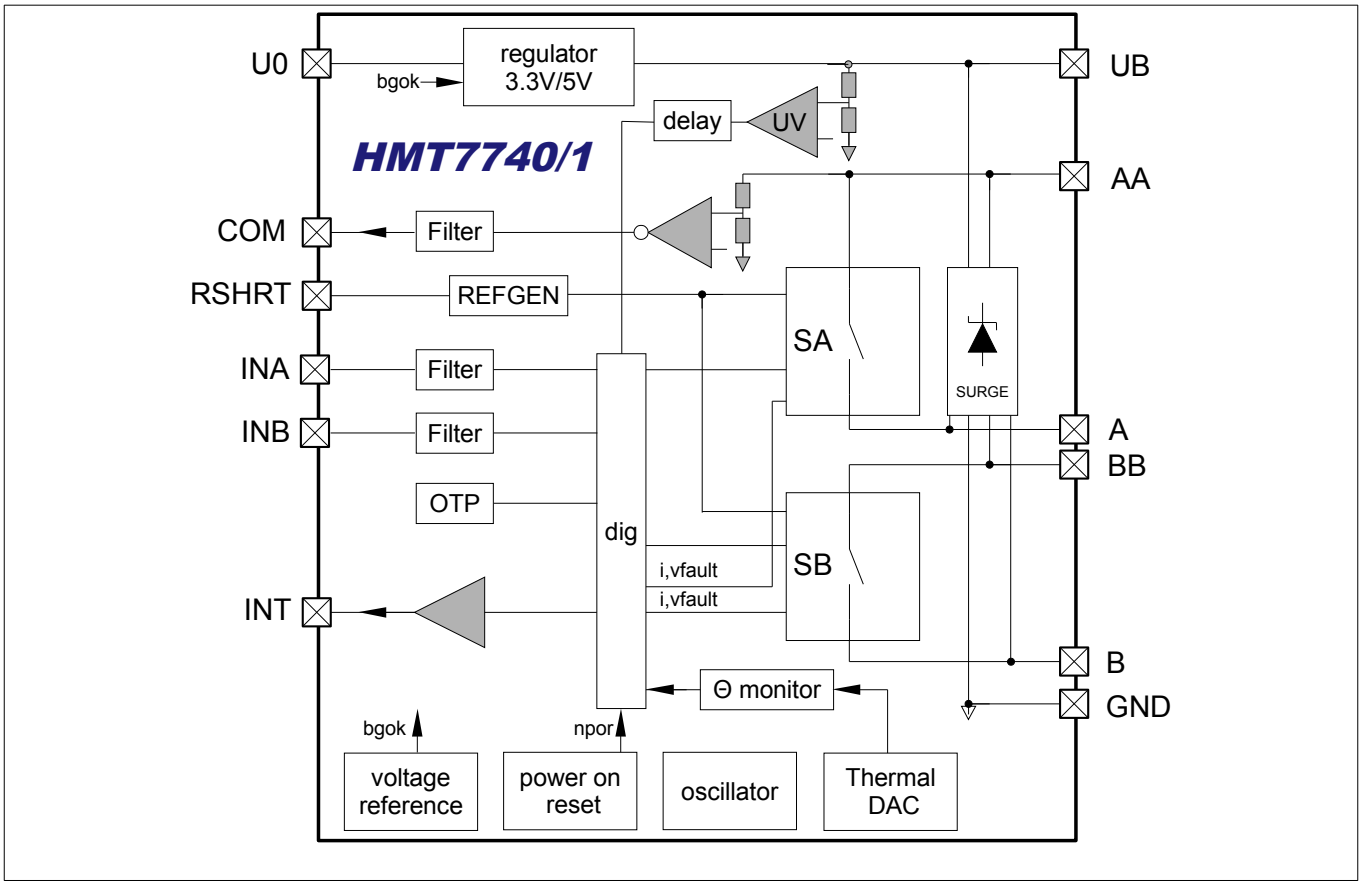
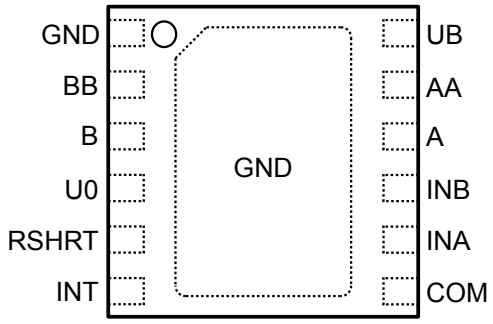


Fig. 1: Block diagram, HMT7740/1

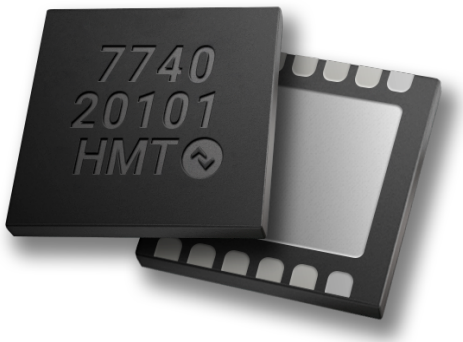
2 Package and pin-out

2.1 DFN 12LD Package - 3mm x 3mm



[Pinout Top View]

NB: GND flag and GND pin to be connected on PCB

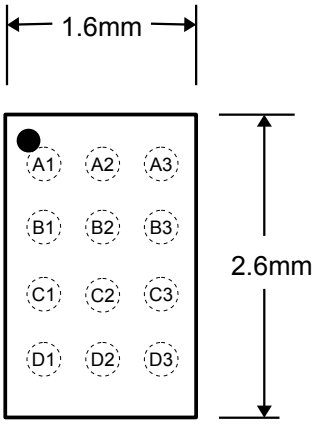


DFN 12LD 3mm x 3mm

Bare die available on request

Fig. 2: Package & Pin-out - DFN

2.2 Chip Scale Package (CSP) - 1.6mm x 2.6mm



[Pinout Top View]

CSP-12 1.6mm x 2.6mm x 0.65mm

HMT7740/1 - CSP Pinout			
Position	Pin	Position	Pin
A1	RSHRT	C1	B
A2	INT	C2	GND
A3	COM	C3	A
B1	U0	D1	BB
B2	INA	D2	UB
B3	INB	D3	AA

Fig. 3: Package & Pin-out - CSP

3 Example Applications

The HMT7740/1 has a highly configurable, fully protected, output stage supporting the following configurations:

- Dual, independent, NPN or PNP channels
- Single output, double drive strength PNP or NPN
- NPN/PNP combinations (e.g. 1xNPN, 1xPNP)
- Push-pull
- Single channel IO-Link configuration
- Dual channel IO-Link configuration

3.1 Example 1 – 1x NPN Boost Mode (parallel switches)

The switches in this example are configured in parallel. This provides a single channel, double drive strength output when more drive capability is required.

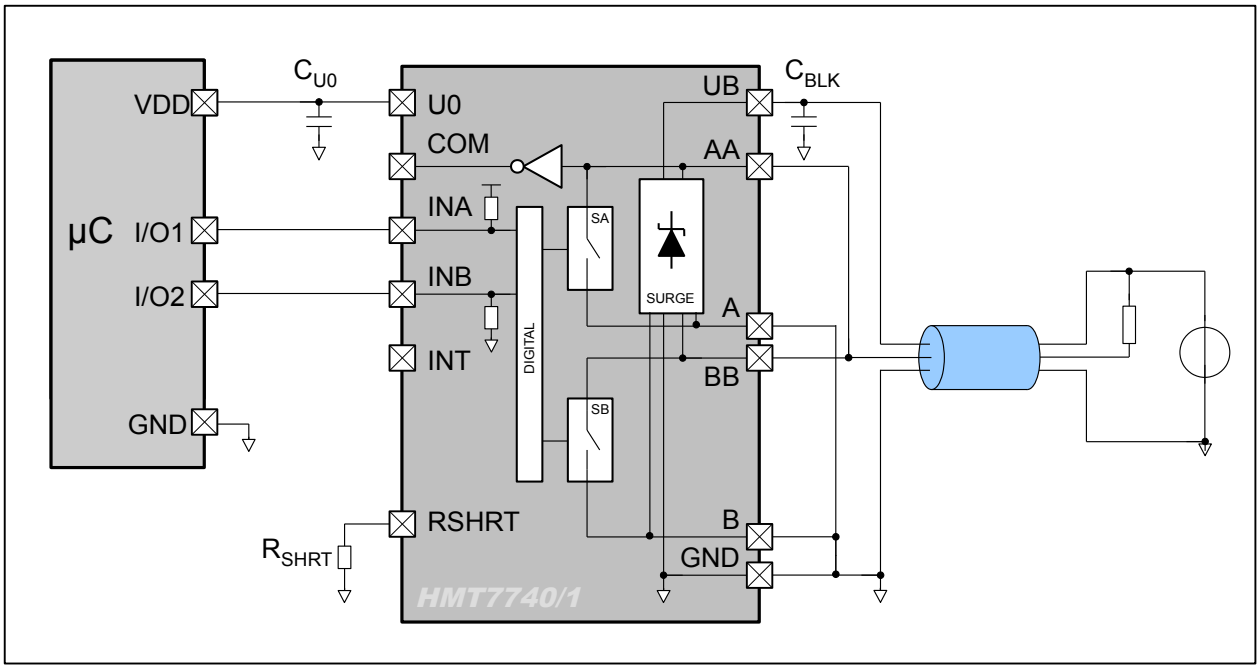


Fig. 4: NPN Boost Mode (parallel switches)

3.2 Example 2 – High side switched coil driver

In this example, the HMT7740/1 is shown to be configured as a coil driver for a valve application. A low-voltage PWM signal is applied to switch input, INA, which controls the coil current. While the PWM signal is active, the low side configured switch, SB, remains closed (D_{FW_EN} active) in order to minimise the voltage drop over the coil, thus improving the efficiency during the off-cycle of the PWM.

A rapid demagnetisation of the coil (fast valve switching) is achieved by opening the switch, SB, when the PWM signal is stopped. This cuts the current path through the free wheeling diode, D_{FW}, thereby providing an alternative path for the current to be rapidly absorbed by the devices robust integrated surge protection.

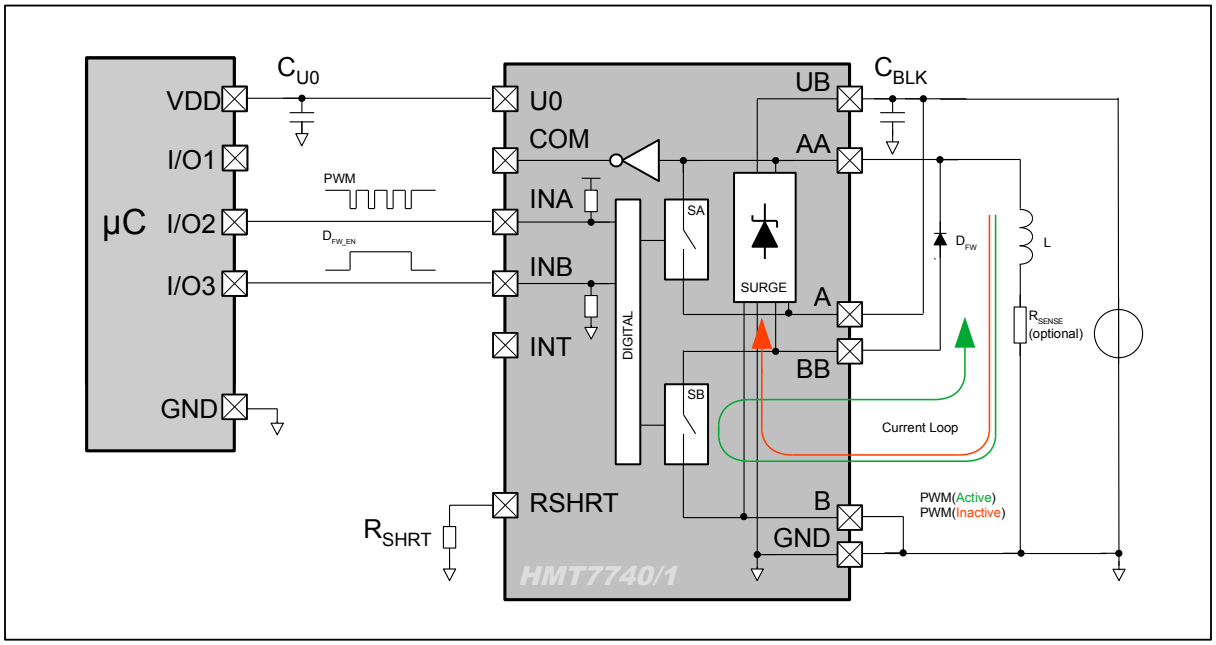


Fig. 5: Coil driver for a valve application

3.3 Example 3 – 1x Push-Pull-HiZ (Single Channel PHY)

The switches in this IO-Link compatible example are configured as a single channel push-pull output. The AA/BB pins combine to form the C/Q channel and are connected to an IO-Link Master. The INA/INB switch control pins are connected together with a capacitor, C_{INAB}, and driven by a microcontroller such that a push-pull-HiZ configuration over a single control line may be realised. The COM and INT pins are monitored by a microcontroller to detect a Wake-up Request (WURQ)[1] or M-Sequence[1] from an IO-Link Master.

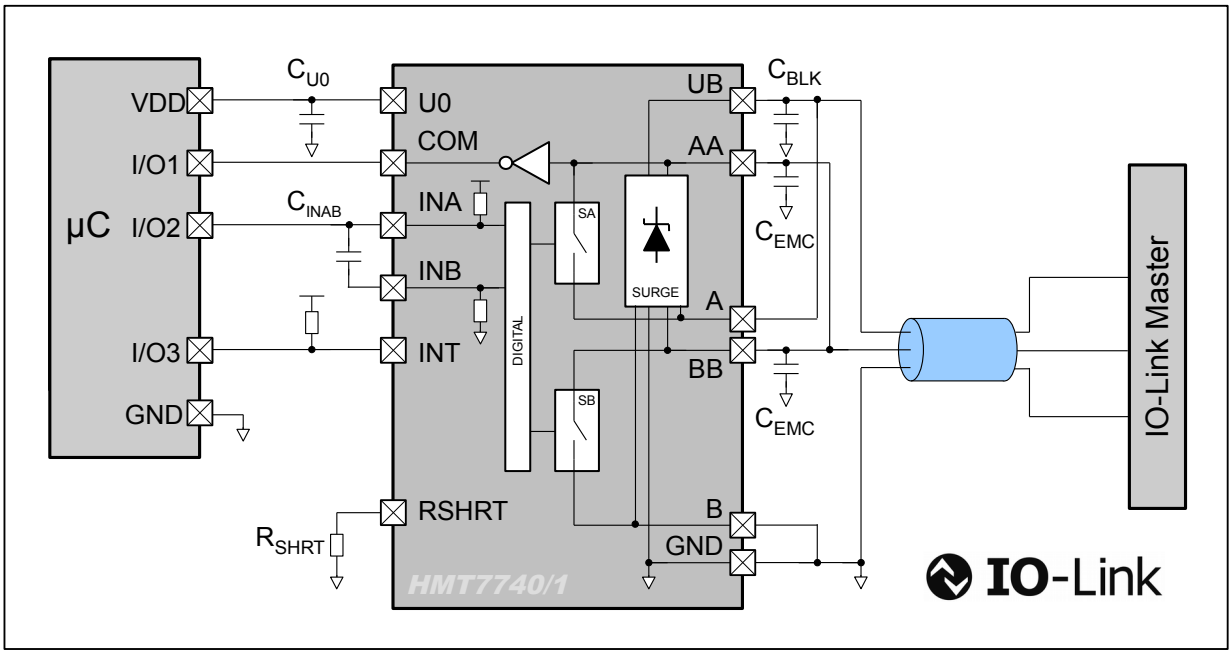


Fig. 6: Push-Pull-HiZ - Single Channel PHY

3.4 Example 4 – 2x PNP (DUAL Channel PHY)

The switches in this IO-Link compatible example are configured as a dual channel PNP output. The AA is the C/Q channel and the BB line the DIO channel. The COM and INT pins are monitored by a microcontroller to detect a WURQ[1] or M-Sequence[1] from an IO-Link Master.

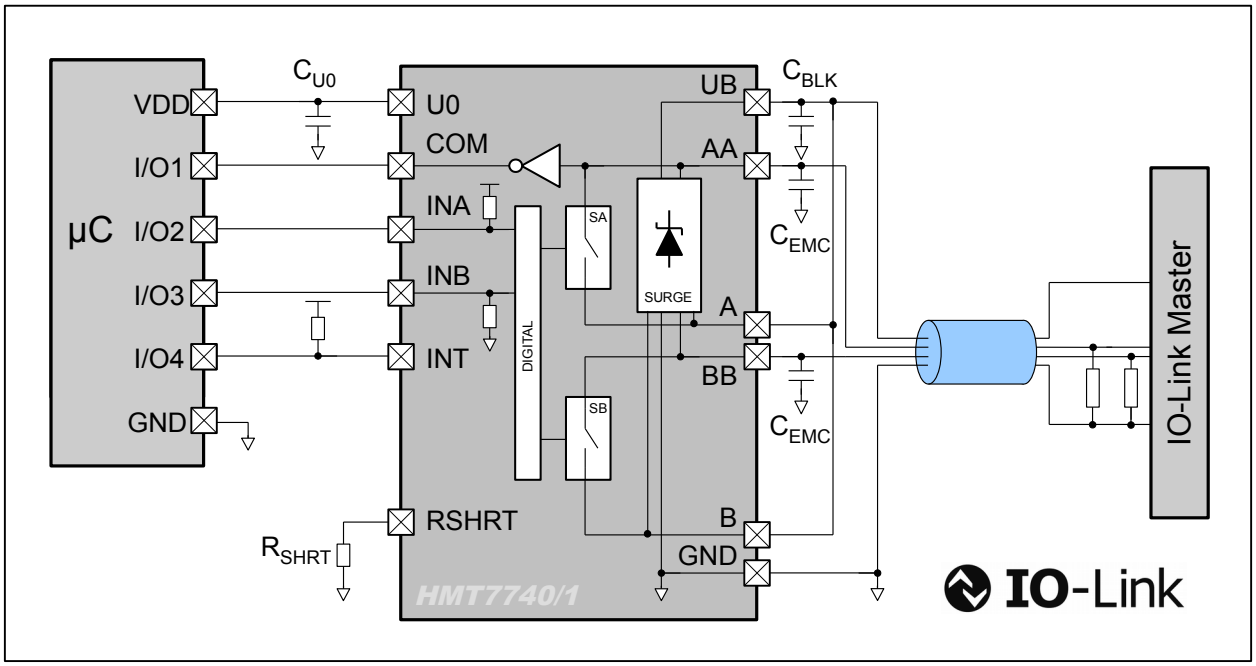


Fig. 7: 2x PNP - IO-Link

4 Functional description

4.1 Start-up

At start-up, power is applied via the cable on UB. A Power On Reset (POR) circuit ensures correct start-up of the HMT7740/1, and that the output switches are initially in a high impedance state.

4.1.1 Example behaviour of the start-up phase

A typical example of the start-up phase is shown in Fig. 8. The supply voltage, UB, in this example reaches the target value rather quickly after connecting the supply cable. The linear regulators output voltage, U0, is somewhat slower to reach the target voltage, since all load capacitances present on the line must first be charged.

At time, $t = t_1$, the linear regulators pseudo band-gap reference voltage is reached which sets the output voltage on U0 close to the target voltage. At time, $t = t_2$, the real band-gap reference voltage is ready to operate and is thus signalled to the linear regulator by setting the BGOK signal to logic level '1'. At this point, the system is fully operational and the regulator completes the start-up phase by setting the output voltage on U0 to the final production trimmed value.

It is important to note that the time difference, $\Delta t = t_2 - t_1$, varies with several parameters, including; process variation, operating temperature, load capacitance and load current. Thus the settling behaviour is subject to variations. However, a proper settling is always ensured.

This output switches, SA and SB, are active at time, t_{DUV}, after the BGOK is set to logic level '1' *and* the UB voltage exceeds the under-voltage threshold, V_{UV}, shown at time, $t = t_3$, in Fig. 8.

At time, $t = t_4$, the supply voltage, UB, begins to drop. It reaches the threshold level, V_{UV}, of the under-voltage detector at $t = t_5$. At this point, the switches are not disabled immediately, as the signal, UV, is delayed by, t_{DUV}. Between time, $t = t_5$ and $t = t_6$, the supply voltage, UB, remains below, V_{UV}, but at a level such that the linear regulator continues to operate, i.e. $\geq UB_{OP}$. At, $t = t_6$, the supply voltage, UB, crosses again the under-voltage threshold, and the process is reversed.

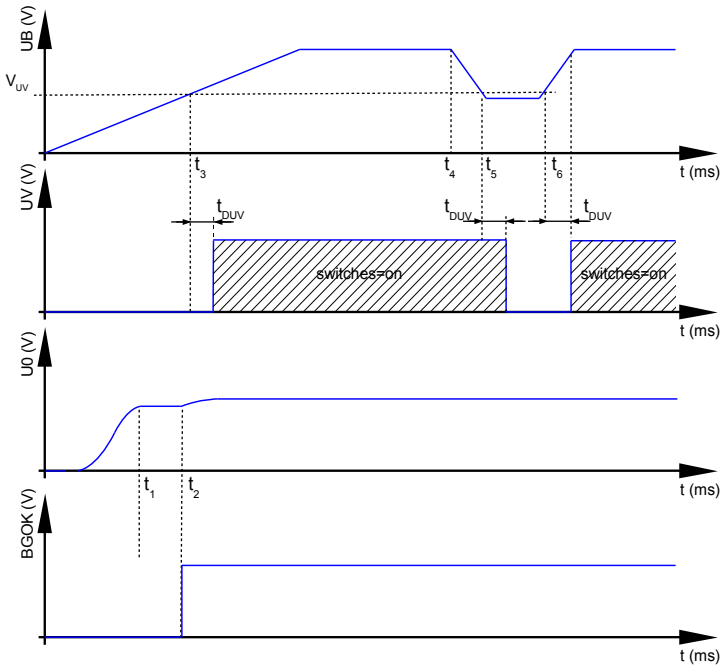


Fig. 8 Example behaviour of a start-up phase

4.1.2 Example behaviour of the shutdown phase

A typical example of the shutdown phase is shown in Fig. 9. In this example the supply voltage, UB, decreases constantly until, $t = t_4$, at which time the voltage falls abruptly to 0V (power supply removed). The several events that occur during this time are described in detail below.

- At time, $t = t_1$, the supply voltage, UB, reaches the threshold voltage of the under-voltage comparator, V_{UV}.

After time, t_{DUV}, the UV signal goes to logic level '0' and the switches, SA and SB are disabled.

- At time, t = t_2, the supply voltage, UB, is below the minimum operating voltage, UB_O, and the output voltage, U0, is no longer able to regulate to the target voltage and instead follows the supply voltage, UB.
- At time, t = t_3, the power-on-reset threshold is reached and the signal NPOR goes to logic level '0'.
- At time, t = t_4, the supply voltage, UB, is 0V and the regulator is no longer operational. The remaining charge stored in the line capacitances are discharged via the load on the line i.e. the application load or the device load itself.
- At time, t = t_5, the band-gap voltage is no longer valid and the BGOK signal goes to logic level '0'.

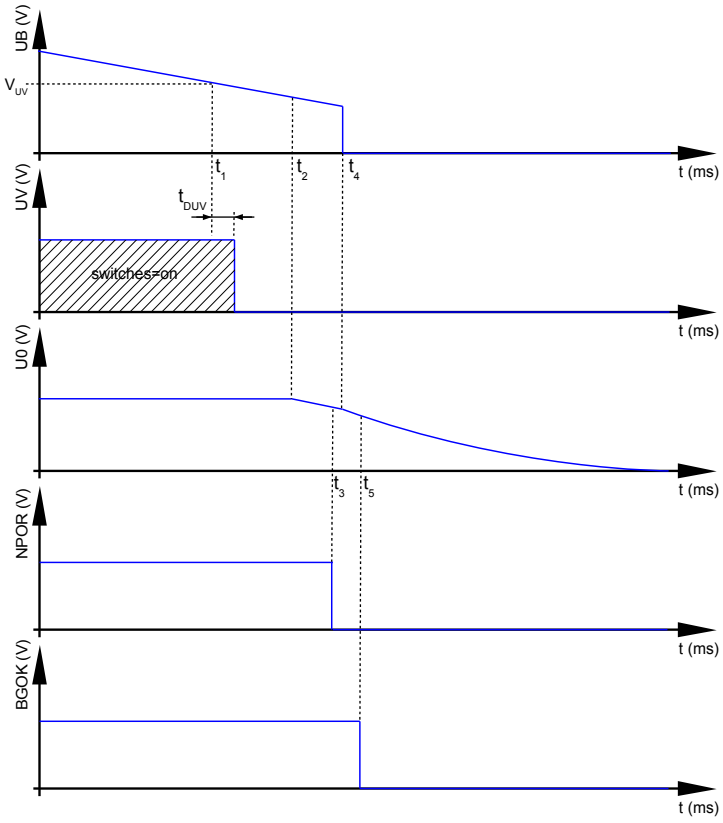


Fig. 9: Example behaviour of a shutdown phase

The application should be designed such that capacitor, C_{U0}, is sufficiently dimensioned to supply the circuit and external loads, such that the output voltage, U0, remains above the POR threshold for the duration of the delay, $t_{DUV,}$ thus ensuring a correct and orderly shut-down procedure.

4.2 Regulator

The device includes a 3.3V (HMT7740) or 5V (HMT7741) linear regulator supplied from the UB pin via an internal reverse protection diode. The linear regulators' output voltage, U0, is given over the entire load rage, I(U0), and requires an external blocking capacitor, $C_{U0,}$ for stable operation.

A maximum static load, equivalent to a resistor, R_{START}, may be drawn externally on U0 during start-up. A static load is the current which would be drawn continuously by the application circuit if the output voltage, U0, were held at a fixed level. A static load in excess of this level may block the start-up.

A higher dynamic load (eg. capacitor charging) is permitted. Dynamic loads will affect (slow) the start, but will not block start-up.

The regulators' dynamic start-up behaviour under different conditions of load capacitance can be seen in Fig. 10. A typical resistive load of 10mA, a supply voltage of 24V with a rise time of 2.4V/µs on pin UB have been used.

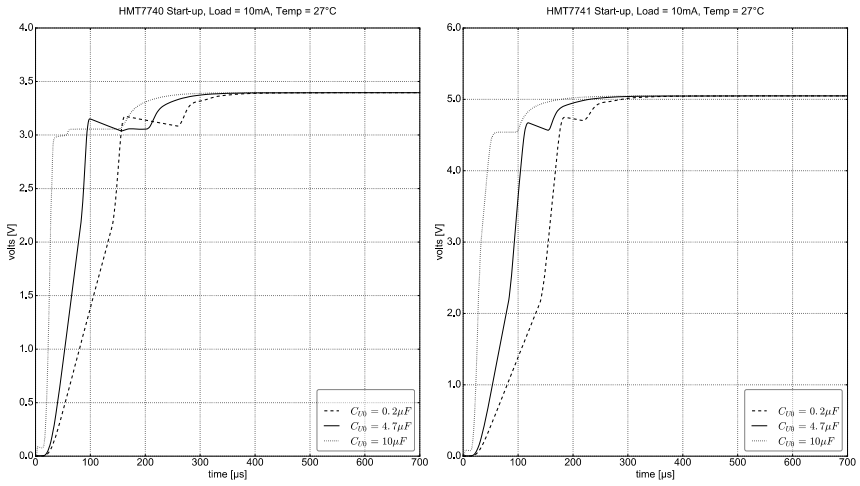


Fig. 10: start-up under different conditions of load capacitance, C_{UO}

4.3 Interrupts on INT pin

An open-drain output (active low) is implemented on the INT pin, and thus, an external pull-up resistor is required. An interrupt is sent on the INT pin whenever a short-circuit condition occurs, that is, when the current flowing in either the SA or SB switch exceeds the short-circuit threshold level, I_{SHRT}, in any direction. See §4.11.

4.4 Digital drive of switches

The switches, SA and BS, are driven by inputs INA and INB respectively. The truth table below shows the four possible combinations.

INA	INB	SA	SB
0	1	ON	ON
0	0	ON	OFF
1	1	OFF	ON
1	0	OFF	OFF

Table 1: Truth table, SA/SB switch control

4.4.1 Majority filter for INA, INB

In order to suppress noise at the input a majority filter is included in the INA and INB signal paths. For the internal state machine to advance, and thus register a valid input signal, a total of five stable samples, measured at a period of T_{INX}, are required. The block diagram is shown in Fig. 11.

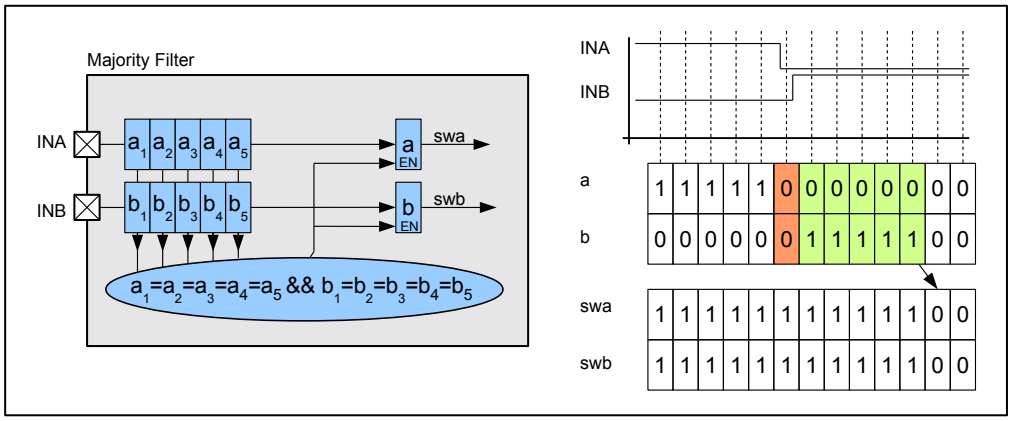


Fig. 11 Majority filter block diagram and principle

An example transition from INA='1', INB='0' to INA='0', INB='1' is shown. INA and INB are sampled on the internal

clock edge at interval T_{INX}, indicated by the dashed lines in the timing diagram. This gives the internally logged values **a** and **b**.

Due to parasitic capacitances present in the application, and to account for different input thresholds due to process variation, INB is shown slightly delayed (nano-seconds) with respect to INA. For a single clock cycle marked in orange, the logged value of ab='00' does *not* correspond to a value intended by the microcontroller.

Only values of a and b are transferred to **swa** and **swb** where **a** and **b** have had the same value for five cycles.

A jitter on pins INA/INB less than $T_{INX(MIN)}$x5 must be assured. The control signals must remain constant for more than $T_{INX(MAX)}$x5 to guarantee a change at the output.

4.4.2 Pull-up and pull-down resistors

The digital inputs, INA and INB, have internal pull-up (R_{PU}) and pull-down (R_{PD}) resistors, respectively. These resistances define the logic state when no micro-controller is present in the application or in the case when the micro-controller is still in a high-impedant state (e.g. at start-up).

With reference to the truth table presented in Table 1, the pull-down resistor, R_{PU}, on input, INB, additionally allows input, INB, to be capacitively coupled to input, INA, with a minimum coupling capacitance of, C_{INAB}, such that a push-pull to HiZ switching sequence may be realised. This simplifies the micro-controller INA/INB driving logic significantly, since only a single control line is required to realise the switching sequence. The value of these resistors is precisely defined in the notes section of §6.3, such that the coupling capacitor, C_{INAB}, may be correctly dimensioned for the application requirements.

4.5 COM comparator output

The voltage level on communication port AA is detected by a resistor divider (nominal resistance R_{IN}) and a comparator with IO-Link compatible thresholds. The COM pin output provides a voltage inversion, if V(AA) rises above the $VinH_{COM}$ threshold the COM pin is at logic level '0', when it falls below $VinL_{COM}$ it changes to logic level '1'.

During start-up, the COM pin is maintained at logic level '1'.

4.5.1 Majority filter

Following the comparator there is a majority filter to suppress noise. Five samples of the comparator output taken at an interval of T_{COM} of the filter are used by a state machine to make the decision.

4.6 Thermal monitor

The HMT7740/1 has an internal 5 bit ADC which is used to measure the die temperature. If the die temperature reaches Θ_2, switches SA and SB are switched to a high impedance state, thereby protecting the device. In an over temperature condition, the threshold is automatically moved to a release threshold Θ_{HYST} below the set point. When the temperature falls below this release threshold, the HMT7740/1 will return to a normal operating state and return the threshold to the original level.

4.7 Under-voltage detector (UV)

An under-voltage condition on UB is detected at a level of $V_{UV.}$ Below this level, switches SA and SB are switched to a high impedance state. §4.1.1 and §4.1.2 describes how this might look in an application during the start-up and shut-down phases, respectively.

The voltage level on UB is detected by a resistive divider (nominal resistance R_{IN}) and a comparator based on the bandgap voltage.

4.8 Switches SA and SB

SA and SB are two independent floating MOS switches which can be operated with current flowing in either direction through the switch. Each switch has an on resistance of R_{SW}.

4.9 Oscillator

An internal oscillator with frequency, f_{CLK}, defines the operating frequencies and delays on the HMT7740/1 device.

4.10 Integrated Surge protection, V_{SURGE}

All high voltage pins (UB, A, B, AA, BB, GND) are protected line-to-line, line to supply and line-to-ground against surges, $V_{SURGE,}$ as defined by the IEC 61000-4-5 standard.

The leakage current of these protections is defined in the electrical parameters (§6.3). A graphical representation of the specified limit for the leakage current is given in Fig. 12. The shaded region represents the limits defined by the electrical parameters, I_{PROTLK} and V_{PROT1}/V_{PROT2} and points 1, 2 and 3 define the test points used in production test.

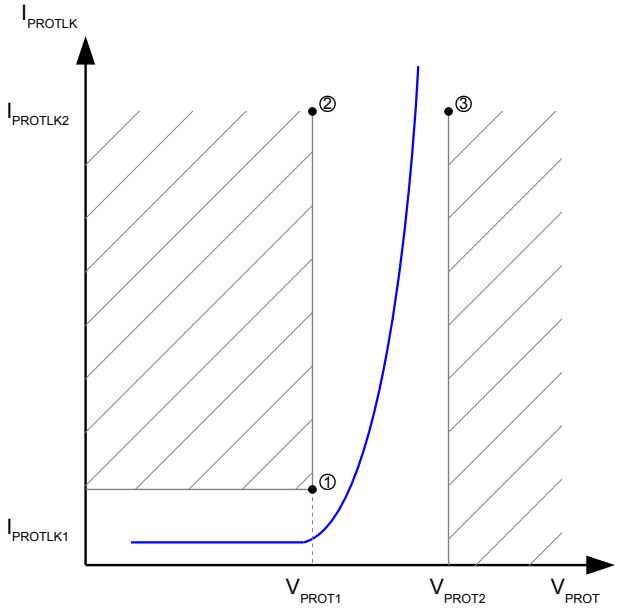


Fig. 12 Leakage current of the surge protection

Notes:

1) point 1 is valid for the entire temperature range
2) leakage currents defined in this chapter refer only to the surge protection circuit. The voltage divider connected to AA used for communication creates an additional current. The equivalent resistance of the voltage divider is given by the parameter R_{IN} defined in chapter 6.3.

4.11 Short circuit detection

The HMT7740/1 includes one short-circuit monitoring block for each output switch, SA and SB, and has the following features:

- hard short circuit mode (disable SA or SB with retry, e.g. IO-Link wake-up request)
- soft short-circuit mode (disable SA or SB without retry, e.g. marginal short circuits)
- configurable thresholds via pin RSHRT
- bi-directional short-circuit detection
- short-circuit threshold derating at higher temperatures

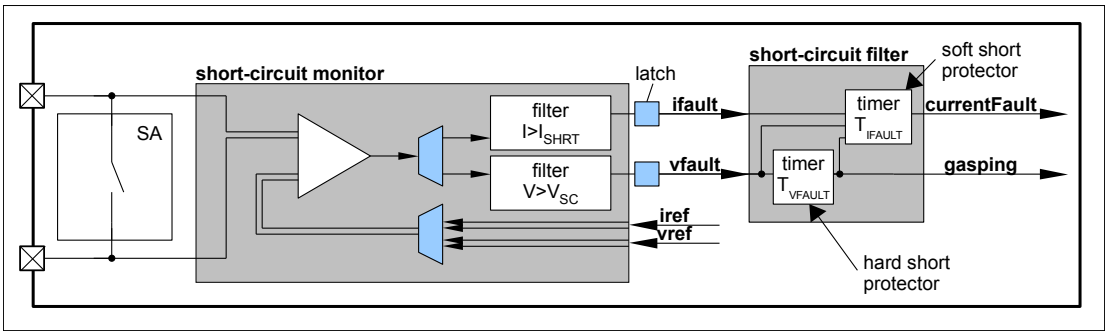


Fig. 13 Short circuit detection architecture. Switch SA shown.

4.11.1 Short circuit monitor

Where an elevated current is passed through either switch, SA or SB, a voltage is developed between the switch

terminals, shown in Fig. 13. This voltage is compared with a selectable threshold in the short-circuit monitor. The selected threshold is rapidly switched to generate a nearly simultaneous comparison at the following two levels:

(1) Soft short-circuit threshold

This threshold is intended to detect a marginal short circuit condition and is set via an external reference resistor on pin RSHRT.

- signal **iref** provides current monitoring, generating signal **ifault**, if $|I_{SWITCH}| > I_{SHRT}$
- The **iref** signal itself is a voltage signal, but creates a valid threshold to determine the switch current as it is derived from the voltage across a matched transistor element, carrying a reference current. See §4.11.5 for further details on the derivation of the I_{SHRT} level.

(2) Hard short-circuit threshold

This threshold is intended for the detection of a hard short-circuit condition such as an IO-Link wake-up request.

signal **vref** provides voltage monitoring, generating signal **vfault**, if $|V_{SWITCH}| > V_{SC}$

The **vref** reference is a fixed voltage based on the bandgap votlage.

4.11.2 Short-circuit filter

The short filter shown in Fig. 13 is a digital block with period T_{IFAULT}. If a short-circuit condition remains active for T_{IFAULT} then the **currentFault** condition is signalled and both switches are disabled. The **vfault** and **ifault** signals from either switch channel are considered equivalent.

In order to provide additional protection in the case of a hard short-circuit, the **vfault** signal is monitored *independently* by the hard short protector. If **vfault** has been continuously active for a period T_{VFAULT}, then the switches are disabled (gasping) for the following period, T_{GASP}. Gasping is considered a short-circuit condition, and the short filter continues to count.

The state of the **vfault** and **ifault** signals are latched when the switches are turned off (INA, INB control signals or thermal shut-down). The short filter continues to count under this condition. This behaviour prevents an erratic input control from defeating the short circuit mechanism. As a result, care must be taken in valve driving applications, such that the peak current during the PWM charging cycle does not exceed the soft short-circuit threshold.

The short circuit filter block, including the latches, are reset on the **allClear** signal provided when the $T_{RESTART}$ timer elapses or the RESURRECT state is entered.

The state machine for the short circuit detection is shown in Fig. 14. Normal operation is state OK, where the switches are active and driven according to Table 1.

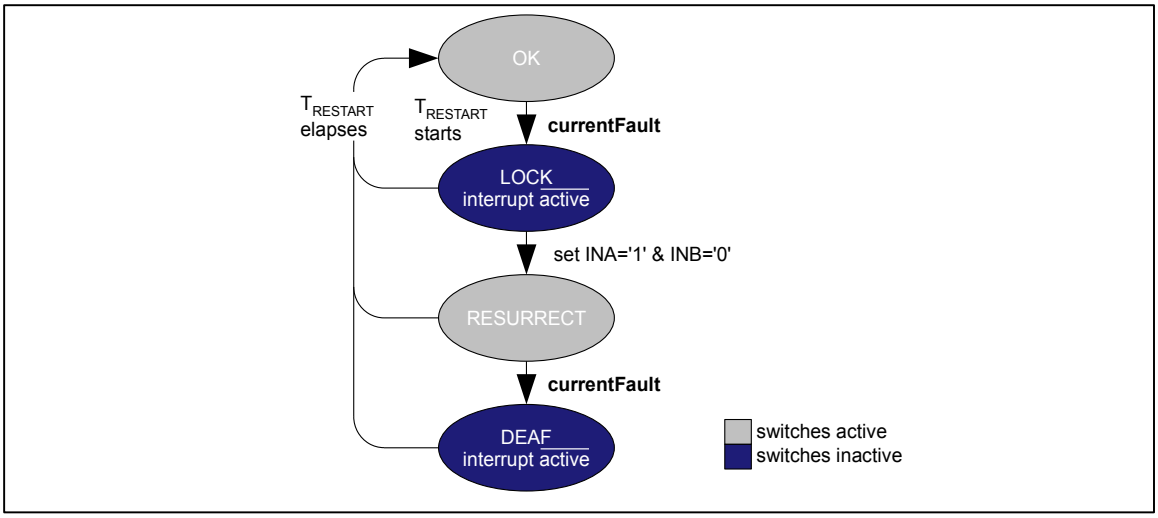


Fig. 14: Short circuit filter state machine

The timing of the short-circuit detection in both hard- and soft short-circuit conditions (i.e. without and without retry, respectively) is such that an IO-Link Wake-up request (WURQ)[1] is correctly detected.

Following a WURQ and accompanying hard short-circuit from a IO-Link master, the currentFault signal is active and the state machine progresses to the LOCK state. As it is necessary to drive the switches again, in order to transmit the device message (M-Sequence)[1] to the IO-Link master, the switch control signals, INA and INB are set to logic level ‘1’ and logic level ‘0’ respectively, which signals to the state machine that it should progress to the

RESSURECT state. In this state the switches are actively driven according to Table 1, and the M-Sequence transmitted to the IO-Link master.

If a further short-circuit condition occurs in the RESSURECT state (currentFault active), the state machine progresses to the DEAF state, where the device forces the switches off, and does not recover until the protective timer, $T_{RESTART}$, has expired. It is therefore not possible for a software fault to cause device damage.

4.11.3 Example behaviour of the short circuit protection

Fig. 15 shows example behaviour of the short-circuit protection under different conditions. In all cases the HMT7740/1 is pulling the AA line high, while the short-circuit is pulling the line low. Contention is shown as an orange band, and a continuing short circuit as a yellow band.

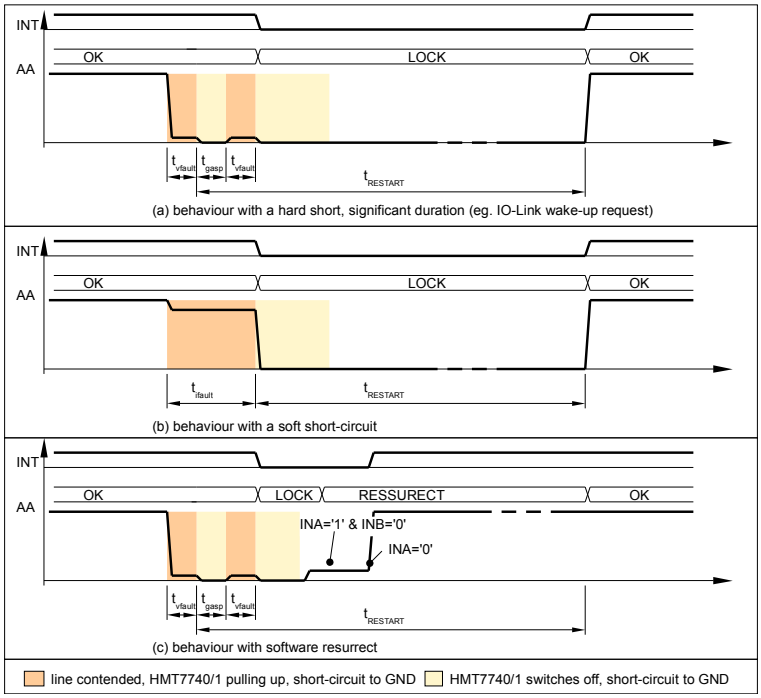


Fig. 15 Example behaviour of the short-circuit protection

4.11.4 Pin RSHRT used as an override input

The short-circuit detection circuitry can be disabled entirely if the voltage on pin RSHRT exceeds V_{REF_RSHRT}. In this mode, the short-circuit state machine (Fig. 14) is placed permanently in the “OK” state, and it is the responsibility of the micro-controller to ensure that device damage from a short-circuit condition does not occur. Fig. 16 shows how the signal “short-circuit override” is generated internally.

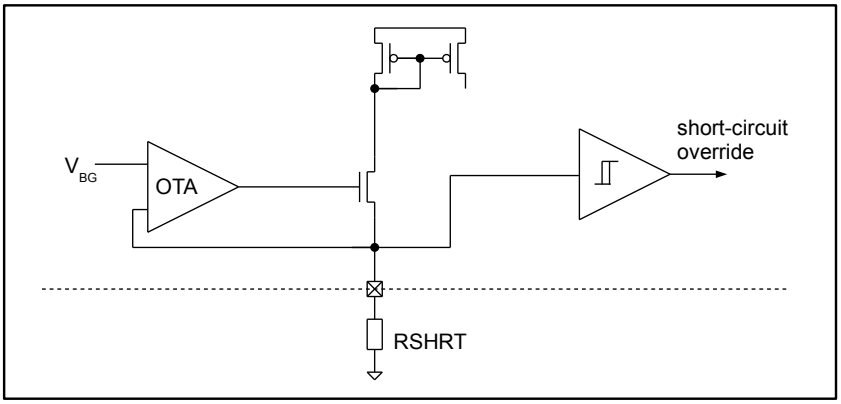


Fig. 16 Pin RSHRT circuitry

4.11.5 Short circuit current derating and REFGEN block

The nominal short-circuit current is set by the resistance connected to the RSHRT pin. From -40°C to Θ_1, the short-circuit is set to its nominal value. Above Θ_1 the short-circuit decreases from its nominal value as shown in

Fig. 17.

The parameters ΔΘ and α are fixed values, thereby giving a fixed slope for the derating. The derating will continue until the thermal shutdown level, Θ_2, is reached, at which point the switches SA and SB are disabled, as described in §4.6.

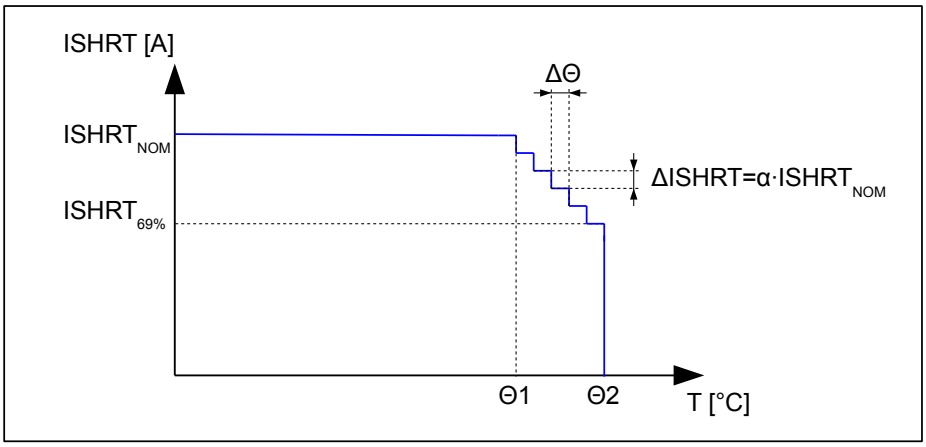


Fig. 17 Short circuit current vs temperature

4.11.6 Choosing RSHRT

R_{SHRT} is chosen according to the application to select the require short-circuit threshold, within the range I_{SHRT}. The resulting short-circuit threshold current is calculated as:

$$I_{SHRT} = \frac{M_{SC} \cdot V_{BG}}{R_{SHRT}}$$

4.12 OTP (one time programmable memory)

An OTP memory is included in HMT7740/1 to allow storage of production trimmed parameters. This memory is not accessible in the application.

4.13 Maximum current output

The switches have a saturation current of I_{SAT}, and will not draw more current than this. If, however, the SA and SB switches are configured to create a single output (double drive strength), then the saturation current in this case will be $2xI_{SAT}$. The power supply must be able to supply this current for the duration $2 \cdot T_{VFAULT}$ to prevent a supply voltage drop on UB.

4.14 Reverse polarity function

When U0 is not supplied (V(UB) ≤ V(GND)) minimal currents, I_{PROTLK}, will flow between any pair of high-voltage pins pins, up to a maximum voltage difference between any pair of pins of 35V.

The regulator is protected from reverse current flow with an internal diode between UB and U0.

4.15 Short term power loss

If the supply on the UB fails then reverse current from U0 to UB is blocked. A residual leakage current of $I_{PLUSREV}$ may still flow in this time. Appropriate dimensioning of the capacitor C_{U0} can be used to maintain the power supply during this event.

4.16 Power Dissipation

The maximum average power consumption in short circuit is:

$$\frac{max(I_{SAT})\cdot max(UB)\cdot T_{VFAULT}\cdot 2}{T_{RESTART}} = 198\,mW$$

The power dissipation into an inductive load, assuming no internal losses in the inductor itself is:

$$f\,\frac{1}{2}L\,I^2$$

Where *f* is the switching frequency, *L* the load inductance and *I* the operating current. The design of the application should take account of this heating.

Fig.18 shows the means to estimate the device junction temperatures based on the dissipation of the regulator and switches.

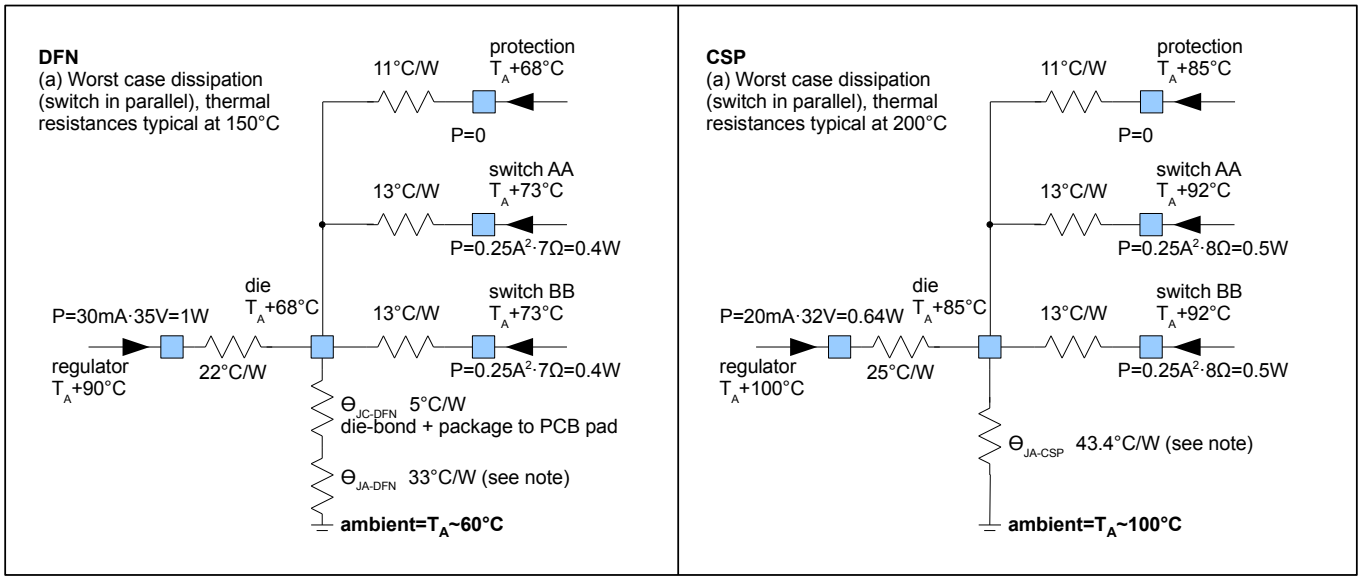


Fig.18 Example thermal power dissipation estimation. Temperatures indicated with respect to ambient.

Note: Since the thermal performance in the final application is dependant on a number of factors (e.g. PCB design, power dissipation of neighbouring components, ambient temperature, air flow. bump-pitch etc), the thermal package properties provided in Fig.18 should only serve as a guideline. The specified values, $\Theta_{JA\text{-}DFN}$ and $\Theta_{JA\text{-}CSP}$, are given based on a four-layer FR-4 PCB, as per JEDEC specification, JESD51-7, under still air conditions.

5 Pins

Pin # DFN	Pin # CSP	Pins	Description	Operation (V)(1)	Type(2)
11	D3	AA	surge protected terminal, switch A	36	ANA IO
10	C3	A	surge protected terminal, switch A	36	ANA IO
2	D1	BB	surge protected terminal, switch B	36	ANA IO
3	C1	B	surge protected terminal, switch B	36	ANA IO
8	B2	INA	logic control, switch A	5	CI, PU
9	B3	INB	logic control, switch B	5	CI, PD
6	A2	INT	short-circuit interrupt indication to µC	5	OD
7	A3	COM	inverting communications input from terminal AA	5	CO
12	D2	UB	positive supply	36	PWR
1	C2	GND	ground supply, reference	ref.	PWR
4	B1	U0	regulated output voltage	3.3/5	PWR
5	A1	RSHRT	connection for resistor to set short-circuit	3.3	ANA I

			level		

Notes:
(1) Indicative only, refer to technical data for specification limits
(2) PWR: power, CI: CMOS input, CO: CMOS output, ANA IO: analog input output, ANA I: analog input, PU: pull-up, PD: pull-down, OD: open drain

Table 2: Device pins

6 Technical Data

6.1 Absolute maximum ratings

	Symbol	Min	Max	Unit
Pin voltage UB		-40	40	V
Pin voltage AA		-40	40	V
Pin voltage BB		-40	40	V
Pin voltage INA, INB and R_{SHRT}		-1	U0+1	V
Storage temperature range before assembly	T_{STOR}	-40	150	°C
Electrostatic device protection (HBM 100pF, 1.5kΩ)	$\|V_{ESD}\|$	4		kV
Electrostatic device protection (machine model)	$\|V_{ESD}\|$	500		V
Soldering temp. (20 – 40 sec.) cf. JEDEC J-STD-020C	T_{LEAD}		260	°C

Notes:

1) All values refer to GND unless otherwise specified.

2) Operation of the device above the absolute maximum ratings may lead to instantaneous device failure. Operation of the device between the operating ratings and the absolute maximum ratings leads to a reduced operating life-time.

Table 3: Absolute maximum ratings

6.2 Operating parameters

	Symbol	Min	Typ	Max	Unit
Operating current supply, no pin currents	I_{QUIES}			2.0	mA
Junction temperature CSP package	$T_{J\text{-}CSP}$	-40		200	°C
Junction temperature DFN package	$T_{J\text{-}DFN}$	-40		150	°C
UB supply voltage, U0=3.3V	UB	5	24	36	V
UB supply voltage, U0=5.0V	UB	7	24	36	V
Continuous regulator load current, pin U0	I(U0)			30	mA
Blocking capacitor on UB	C_{BLK}	100			nF
U0 blocking capacitor (no minimum ESR)	C_{U0}	0.2	1	10	µF
Load capacitor on AA and BB	C_{LOAD_MAX}			500	nF
EMC capacitor, C_{EMC}	C_{EMC}		470		pF
INA-INB coupling cap. Single drive push-pull conf.	C_{INAB}	220			pF
Short-circuit set resistor	R_{SHRT}	12		39	kΩ

Table 4: Operating parameter

6.3 Electrical parameters

Electrical parameters are valid over the operating temperature ($T_{J\text{-}DFN}$, $T_{J\text{-}CSP}$) and voltage range, unless otherwise explicitly stated.

Parameter	Test conditions, comment	Symbol	Min	Typ	Max	Unit
Oscillator						
Internal clock base		f_{CLK}	-10%	10	+10%	MHz
Voltage reference						
Band-gap voltage		V_{BG}	-6%	1.23	6%	V
Short circuit						
Soft short-circuit current	R_{SHRT}=12kΩ	I_{SHRT}	249	279	309	mA
	R_{SHRT}=22kΩ		125	155	185	
	R_{SHRT}=39kΩ		57	87	117	
Short-circuit multiplier		M_{SC}		2770		
Hard short-circuit limit		V_{SC}	2.8		7	V
Hard short-circuit filter	f_{CLK}=10MHz	T_{VFAULT}		20		µs
Soft short-circuit filter	f_{CLK}=10MHz	T_{IFAULT}		60		µs
Retry gap	f_{CLK}=10MHz	T_{GASP}		20		µs
Short circuit restart	f_{CLK}=10MHz	$T_{RESTART}$		19.7		ms
Threshold for logic high	pin RSHRT	V_{REF_RSHRT}	0.7xV(U0)			V
Derated temperature		Θ_1	129	135	141	°C
Shutdown temperature		Θ_2	169	175	181	°C
LSB short-circuit derating		α		1/14		-
LSB for the temperature		ΔΘ		8		°C
Over-temp. hysteresis		Θ_{HYST}		8		°C
Regulator						
Output capability	3.3V or 5.0V	I(U0)			30	mA
Startup static capability	3.3V	$R_{START3V3}$	67			Ω
	5.0V	$R_{START5V0}$	160			Ω
Operating voltage	I(U0) ≤ 25mA	UB_{OP1}	U0+1.7V		36	V
Operating voltage	I(U0) ≤ 30mA	UB_{OP2}	U0+2.0V		36	V
Regulator output voltage	3.3V variant, HMT7740	U0	-5%	3.3	5%	V
Load regulation (DC)	1mA < I(U0) ≤ 30mA	ΔU0			50	mV
Line regulation (DC)	UB=10-36V	ΔU0			10	mV
Temperature variation	I(U0)=15mA, UB=24V	|ΔU0|			50	mV
Regulator output voltage	5.0V variant, HMT7741	U0	-5%	5.0	5%	V
Load regulation (DC)	1mA < I(U0) ≤ 30mA	ΔU0			50	mV
Line regulation (DC)	UB=10-36V	ΔU0			10	mV
Temperature variation	I(U0)=15mA, UB=24V	|ΔU0|			50	mV
Back current	UB=0V, U0=3.3V	$I_{PLUSREV}$			10	µA
Power supply ripple rejection at U_B≥ 10V,	C_{U0}=1µF, I(U0)=1-10mA f < 1kHz	PSRR	70			dB

Parameter	Test conditions, comment	Symbol	Min	Typ	Max	Unit
U_O=3.3V	f = 1kHz-500kHz f > 500kHz		35 50			
Power supply ripple rejection at U_B≥ 7V, U_O=3.3V	C_{U0}=1µF, I(U0)=1-10mA f < 1kHz f = 1kHz-500kHz f > 500kHz	PSRR	 60 30 40			dB
Power supply ripple rejection at U_B= 5V, U_O=3.3V	C_{U0}=1µF, I(U0)=1mA f < 1kHz f = 1kHz-500kHz f > 500kHz	PSRR	 43 24 50			dB
Power supply ripple rejection at U_B= 5V, U_O=3.3V	C_{U0}=1µF, I(U0)=10mA f < 1kHz f = 1kHz-500kHz f > 500kHz	PSRR	 39 21 38			dB
Power supply ripple rejection at U_B≥ 10V, U_O=5.0V	C_{U0}=1µF, I(U0)=1-10mA f < 1kHz f = 1kHz-500kHz f > 500kHz	PSRR	 70 35 50			dB
Power supply ripple rejection at U_B≥ 7V, U_O=5.0V	C_{U0}=1µF, I(U0)=1-10mA f < 1kHz f = 1kHz-500kHz f > 500kHz	PSRR	 52 22 39			dB
POR						
POR release threshold		V_{POR}	1.6		2.7	V
POR hysteresis		V_{HYST}	0.05	0.2	0.3	V
Output switches						
Output resistance	I_{LOAD}=200mA	R_{SW}	2	3.5	8	Ω
Tolerance	I_{LOAD}=200mA @ 24°C	R_{SW_TOL}	-20	3.5	20	%
Switching transition	C_{BLK}>10nF, 10%-90%, UB=24V	t_{SW}			1	µs
IN pin filter sample period	f_{CLK}=10MHz	T_{INX}		0.1		µs
Saturated current		I_{SAT}	0.75	1.7	2.7	A
Line surge protection, parameters with respect to any pair AA, BB, UB, GND, A, B						
Protection leakage	V=±36V	$I_{PROTLK2}$			100	µA
	V=±36V < 150°C	$I_{PROTLK1}$			10	µA
Protection threshold	I=0.1A	V_{PROT1}	39	42	45	V
Protection threshold	I=2A	V_{PROT2}		45		V
Surge Protection	IEC 61000-4-5 (±1kV/500Ω 1.2µs/50us)	V_{SURGE}		±1		kV
Under-voltage detector						
Under-voltage detect	U0=3.3V	V_{UV}	4.5	5	5.5	V
Under-voltage detect	U0=5.0V	V_{UV}	6.3	7	7.7	V
Under-voltage delay		t_{DUV}		100		µs
Digital pins: INA, INB, INT and COM						
Output pin current	ΔV=0.5V	I_{DIG}	4			mA
Input low signal		V_{DL}	-0.5		0.15V_{U0}	V

Parameter	Test conditions, comment	Symbol	Min	Typ	Max	Unit
Input high signal		V_{DH}	$0.5V_{U0}$		V_{U0}+0.5	V
Pull-up of INA and pull-down of NB (1)		R_{PU}/R_{PD}	50	100	200	kΩ
Leakage current of INT	No resistor connected to the output	$I_{LEAK(INT)}$			10	µA
Communication Port AA, according to IO-Link standard [1] UB > 18V, unless otherwise specified						
Input Threshold High		$VinH_{COM}$	10.5		13	V
Input Threshold Low		$VinL_{COM}$	8		11.5	V
Input Threshold Hysteresis (High-Low)		Vin_{HYST}		1		V
Input resistance		R_{IN}	2.2	4.5	8.6	MΩ
COM pin filter sample period	f_{CLK}=10MHz	T_{COM}		0.1		µs

Notes:

(1) the R_{PU}/R_{PD} resistances have an approximate nominal process variation of +35% / -31% The temperature variation is given by the following approximation:

$$R_\theta = R_{\theta_{NOM}} \cdot \left(1 \cdot 10^{-5} \cdot \theta^2 - 0.0034 \cdot \theta + 1\right)$$

For example, at 150°C the resistance is equal to:

$$R_{150\,^\circ C} = 100\,k\Omega \cdot \left(1 \cdot 10^{-5} \cdot 150^2 - 0.0034 \cdot 150 + 1\right) \approx 80\,k\,\Omega$$

Fig. 19 shows the temperature behaviour of the normalised resistance between -50° and 200°C.

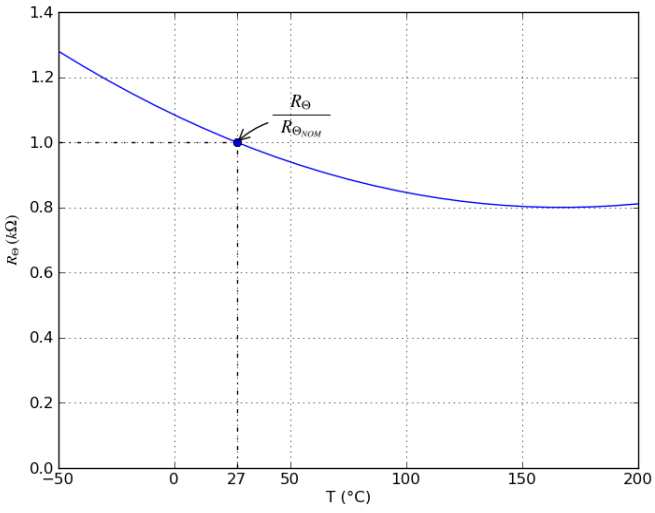
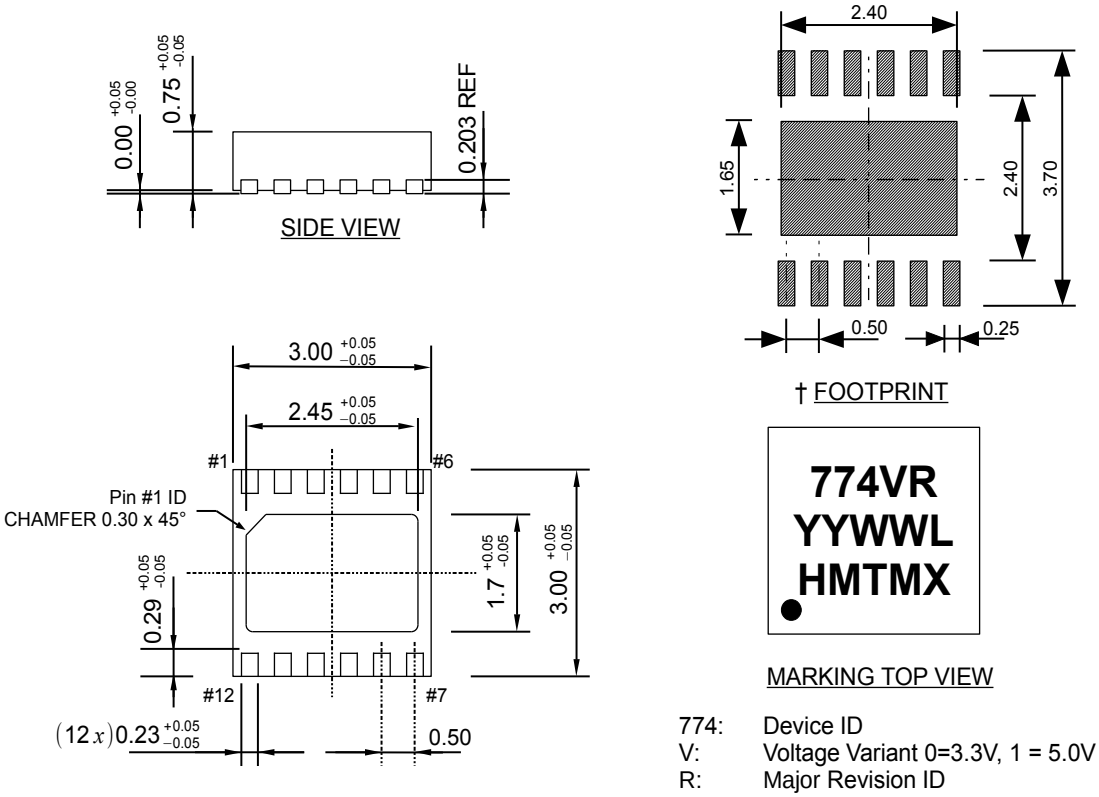


Fig. 19: Temperature behaviour of the pull-up and pull-down normalised resistance.

7 Packaging



774:	Device ID
V:	Voltage Variant 0=3.3V, 1 = 5.0V
R:	Major Revision ID
YY:	Year code
WW:	Week code
L:	Lot in week
HMT:	HMT fixed string
M:	Minor Revision ID
X:	Internal use

NOTES:

All measurements are in millimeters

† suggested footprint for high density PCB design. Multiple vias from flag to extended internal plane required for correct thermal performance.

Fig. 20 Package and footprint drawing - DFN12

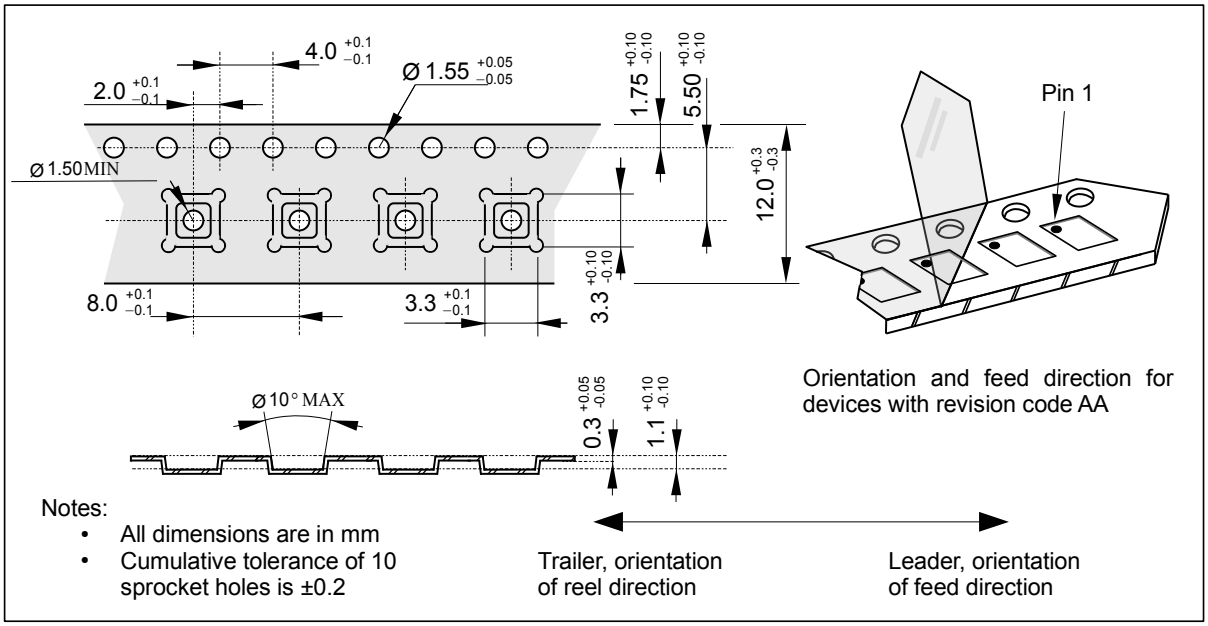
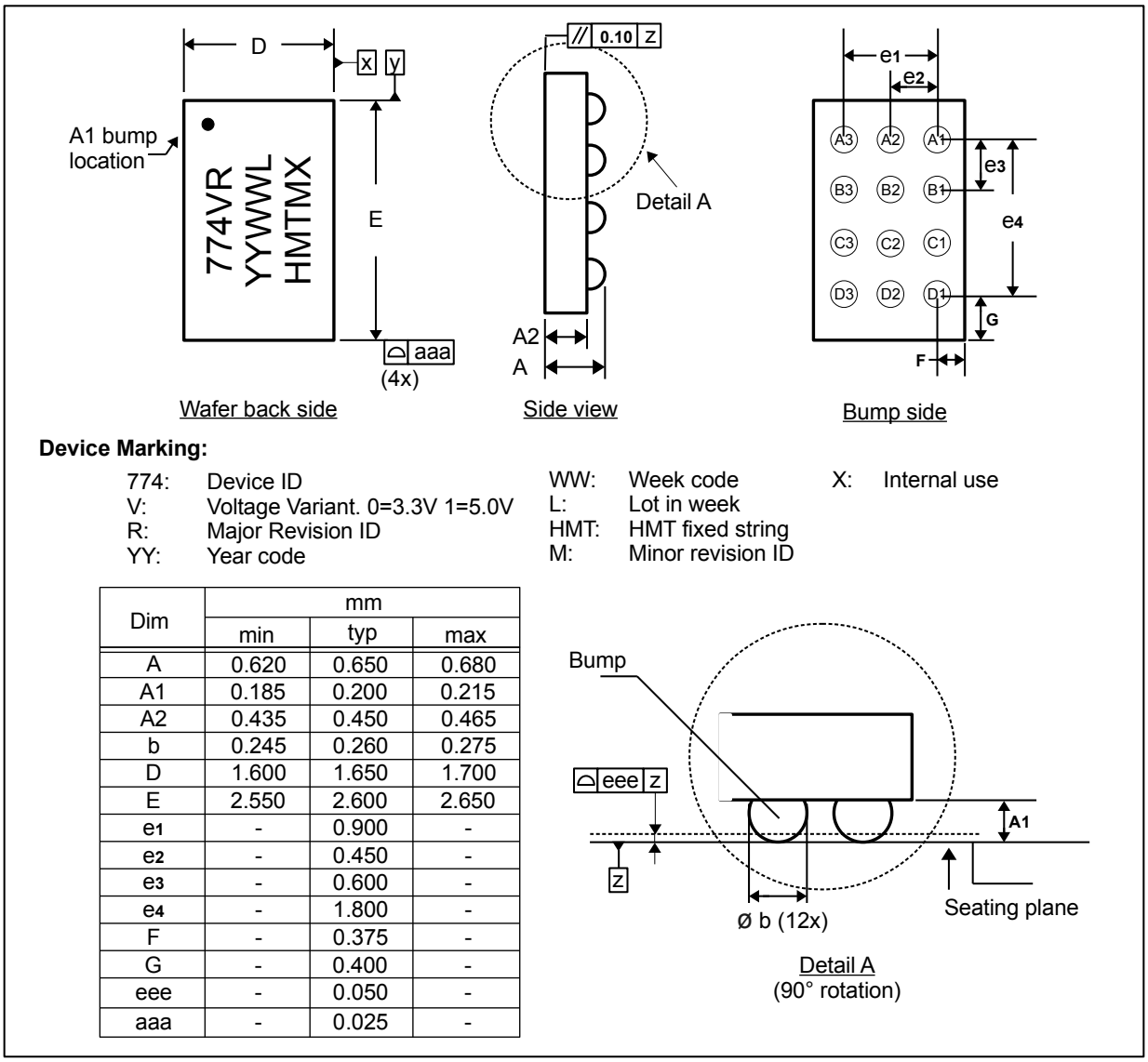


Fig. 21 Tape & Reel Specification - DFN12

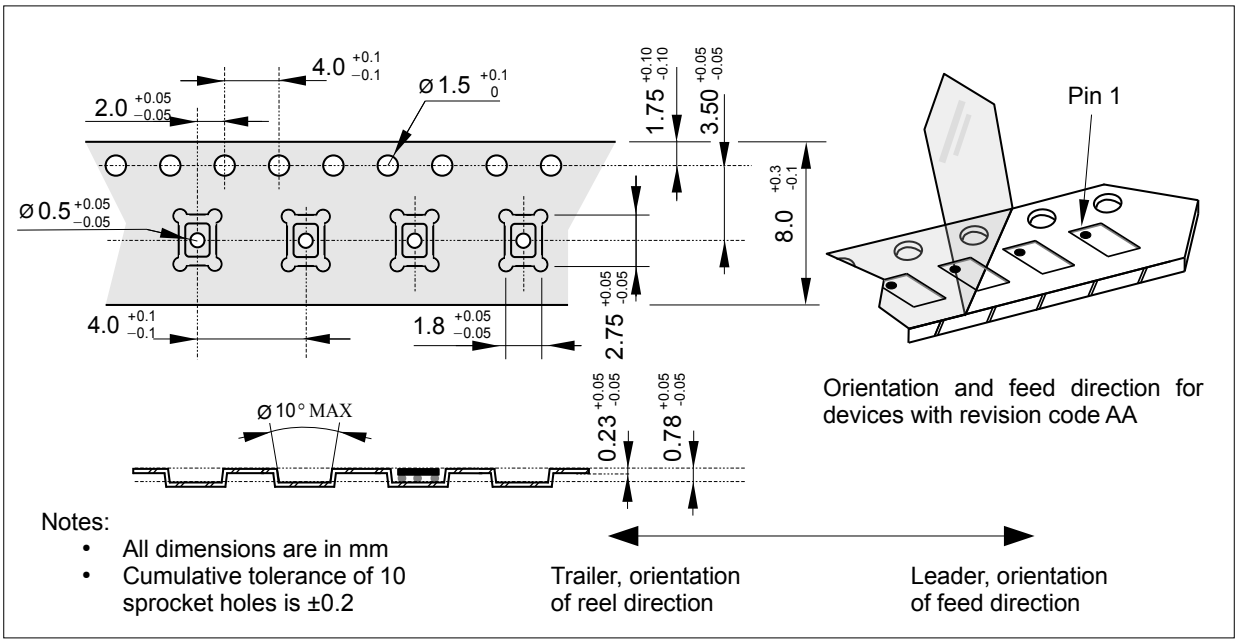


Device Marking:

774:	Device ID	WW:	Week code	X:	Internal use
V:	Voltage Variant. 0=3.3V 1=5.0V	L:	Lot in week		
R:	Major Revision ID	HMT:	HMT fixed string		
YY:	Year code	M:	Minor revision ID		

Dim	mm		
	min	typ	max
A	0.620	0.650	0.680
A1	0.185	0.200	0.215
A2	0.435	0.450	0.465
b	0.245	0.260	0.275
D	1.600	1.650	1.700
E	2.550	2.600	2.650
e1	-	0.900	-
e2	-	0.450	-
e3	-	0.600	-
e4	-	1.800	-
F	-	0.375	-
G	-	0.400	-
eee	-	0.050	-
aaa	-	0.025	-

Fig. 22 Package drawing - CSP



Notes:

- All dimensions are in mm
- Cumulative tolerance of 10 sprocket holes is ±0.2

Fig. 23: Tape & Reel Specification - CSP